AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

Claims 1-11 (cancelled)

12. (Original) A semiconductor device comprising:

a plurality of word lines, a plurality of data lines, and a plurality of DRAM memory cells;

a plurality of sense amplifiers coupled to said plurality of data lines and each receiving operating voltage from first and second nodes;

a first line connected to said first nodes;

a second line connected to said second nodes;

first drive means coupled to said first line;

second drive means coupled to said second line;

wherein each of said plurality of sense amplifiers includes a NMISFET pair arranged in a cross-coupled form and a PMISFET pair arranged in a cross-coupled form,

wherein said first drive means sets said first line to have a first potential, a second potential, a third potential between a row active command and a precharge command,

wherein said second drive means sets said second line to have a fourth potential, a fifth potential, a sixth potential between said row active command and said precharge command,

wherein after said row active command is issued, said first drive means drives said first line to said first potential and then to said second potential, and before said precharge command is issued, said first means drive drives said first line from said second potential to said third potential,

wherein said second potential is lower than said first potential, and is higher than said third potential,

wherein after said row active command is issued, said second drive means drives said second line to said fourth potential and then to said fifth potential, and before said precharge command is issued, said second drive means drives said second line from said fifth potential to said sixth potential, and

wherein said fifth potential is higher than said fourth potential, and is lower than said sixth potential.

13. (Original) The semiconductor device according to claim 12,

wherein said first drive means drives said first line to said first potential in response to a first signal, and drives said first line from said second potential to said third potential in response to a second signal.

14. (Original) The semiconductor device according to claim 13,

wherein said second drive means drives said second line to said fourth potential in response to a third signal, and drives said second line from said fifth potential to said sixth potential in response to a fourth signal.

15. (Original) The semiconductor device according to claim 14,

wherein said first line is coupled to said PMISFET pairs, and

wherein said second line is coupled to said NMISFET pairs.

16. (Original) The semiconductor device according to claim 14,

wherein a voltage level of said third signal is the same as a voltage level of a word line when selected.

17. (Original) The semiconductor device according to claim 15,

wherein said first drive means includes a first PMISFET having its source/drain path between said first line and the second potential,

wherein said second drive means includes a first NMISFET having its source/drain path between said second line and the fifth potential,

wherein a gate of said first PMISFET receives said second signal, and

wherein a gate of said first NMISFET receives said fourth signal.